Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claims 1-11 (cancelled)

Claim 12 (new): A method for accessing a dynamic random access memory (DRAM), the DRAM having a plurality of memory storage elements located in rows and columns, the method comprising steps of:

a) initiating a first memory access by providing a first address signal indicative of the location of at least one memory storage element to be accessed;

b) decoding the first address signal to select a row and at least one column corresponding to the location of the at least one memory storage element;

c) enabling a word line corresponding to the selected row;

d) activating a sense amplifier to latch data to or from the at least one selected column;

e) disabling the word line corresponding to the selected row;

f) precharging the at least one selected column;

g) initiating a second memory access by providing a second address signal indicative of the location of at least one memory storage element to be accessed; and

h) decoding the second address signal to select a row and at least one column corresponding to the location of the at least one memory storage element, the second memory access commencing before the step of precharging the selected column has completed.

Claim 13 (new): A method according to claim 12, wherein the step of decoding the second address signal occurs at substantially the same time as the precharging step.

Claim 14 (new): A method according to claim 12, wherein the memory storage elements are arranged in a plurality of sub-arrays and the method further comprises decoding the first and second address signals to select at least one sub-array.

Claim 15 (new): A method according to claim 12, wherein decoding the first address signal comprises decoding a row address and a column address at substantially the same time.

Claim 16 (new): A method according to claim 12, wherein decoding the second address signal comprises decoding a row address and a column address at substantially the same time.

Claim 17 (new): A method according to claim 12, wherein the memory access is one of a read access, a write access, or a refresh access.

Claim 18 (new): A method according to claim 12, including the step of deriving a plurality of self timed clock pulses from a system clock signal for controlling the timing of steps (b) to(f).

Claim 19 (new): A method according to claim 12, including the step of performing memory accesses on consecutive cycles of a system clock signal.

Claim 20 (new): A dynamic random access memory (DRAM) comprising:

a) a plurality of memory storage elements located in rows and columns, each memory storage element being coupled to a bit line and a word line;

b) a row decoder for decoding a row address from an address signal and for asserting a word line signal on a word line corresponding to the decoded row address;

c) a column decoder for decoding a column address from the address signal and for selecting at least one bit line;

d) precharge circuitry for precharging the at least one bit line; and

timing circuitry for controlling the activation of the precharge circuitry such that the precharging occurs at substantially the same time as the address signal is being decoded by the row and column decoders.

Claim 21 (new): A DRAM according to claim 20, wherein the memory storage elements are arranged in a plurality of sub-arrays, the DRAM further comprising a sub-array decoder for decoding the address signal to provide a sub-array select signal.

Claim 22 (new): A DRAM according to claim 21, wherein each sub-array comprises a data line, the data line capable of being coupled to the selected bit line.

Claim 23 (new): A DRAM according to claim 20, wherein the DRAM is an embedded DRAM macrocell.

Claim 24 (new): A DRAM according to claim 20, further comprising an address register for latching the address signal in response to a system clock signal.

Claim 25 (new): A DRAM according to claim 20, wherein the decoded row address is combined with a word line timing pulse to assert the word line signal on the word line.

Claim 26 (new): A DRAM according to claim 20, wherein the timing circuitry comprises a delay element that is used to provide a time delayed version of a system clock signal for synchronizing the activation of the precharge circuitry.

Claim 27 (new): A DRAM according to claim 20, wherein the address signal comprises N bits defining the column address and M bits defining the row address.

Claim 28(new): A DRAM according to claim 20, wherein the row decoder and the column decoder decode the address signal at substantially the same time.